Design of the differential chaos shift keying communication system based on DSP builder

Zhiping Liu[1*], Jinhua Zhang[2], Hanyu Liu[1]

[1]*School of Electrical Engineering and Automation, Henan Polytechnic University, Jiaozuo, China, 454000*

[2]*Beijing Ripeness Sanyuan Instrumentation CO. LTD, Beijing, China, 100027*

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Abstract

Chaotic communication has the good secrecy. It is an important branch of the modern secure communication. Differential chaos shift keying (DCSK) communication system adopts shift keying to separate the reference signal and data signal. It has a strong resistance to the multipath channel. For FPGA systems design shortcomings using a hardware description language directly, the DCSK communication system is proposed in DSP Builder software method. The simulation results show the correctness of the design system. The DSP Builder platform can be linked with FPGA seamlessly. It makes the development convenient for chaotic communication system design based on FPGA, and the designed DCSK communication system has practical value.

Keywords: chaotic communication, differential chaos shift keying, DSP builder, FPGA, logistic map

1 Introduction

The study of chaos theory has always been given great concern, since the Lorenz discovered the chaos phenomenon. With the deepening research of chaos, it presents and has been widely used in many areas of engineering, and these areas of application are inseparable from the theory of chaotic systems. There are a variety of models for chaotic systems, such as Lorenz system and the Henon system with more precise mathematical model. Then some scholars have a more detailed analysis and simulation of these systems, the literature [8] is a theoretical and experimental analysis of the Lorenz system and Chua's circuit chaotic mechanism, and some other scholars carried out a detailed study of the generation of it by entity analog circuit, the literature [9] is the experimental study of the chaotic source through entities analog circuits.

In the study of chaos, the chaos system designed by analog circuits is not only with high cost but relatively less stable and vulnerable to the impact of the external factors, which will restrict the study of it and place much difficulty on its practical application. The research based the chaos in the field of communication, is the very important research direction in recent years. When the signal transmits in the air, it should particularly take the anti-interference performance of the transmission signal into consideration, which requires researchers to put forward more new methods, in the past some scholars have introduced digital system model into this field, which also makes a great step forward to the practical application of chaos in communications.

The DSP Builder of Matlab/Simulink is a system-level design tools to help designers to complete the DSP system design based on FPGA. It is based on a number of software tools and can connects the design tools of system-level and RTL level to maximize the advantages of the two tools, which will bring shorter development cycles and higher efficiency to the digital systems based on it.

Concerning of the drawbacks of past physical analogue circuit implementation, the disadvantages of longer development cycles and lower efficiency of the chaos system based on the digital system model the past, and the shortages of FPGA systems designed directly using the hardware description language, the paper attempts to propose a new method to complete the chaotic system based on DSP Builder in the communication system.

2 Logistic map

In chaotic systems, because of its sensitive dependence on initial value, for different initial conditions, as long as the observation time is long enough, the movement of the dissipative system in the phase space will shrink to a limited area. It is the basic reference conditions to test a chaotic systems. Here we use the logistic system as an example to study, Logistic system Equation is:

$x_{n+1} = ax_n(1-x_n)$, n =0,1,2,…; (a - scale factor)

Figures 1, 2, 3 Phase diagram Analysis with Matlab/ Simulink.

It can be seen from Figure 1, Figure 2, Figure 3, small changes of the a parameter will cause huge changes in results, and this is its initial value sensitivity, then there has a great practical significance to the research of Logistic system.

[*]***Corresponding author's*** e-mail: liuzhipinghpu@163.com

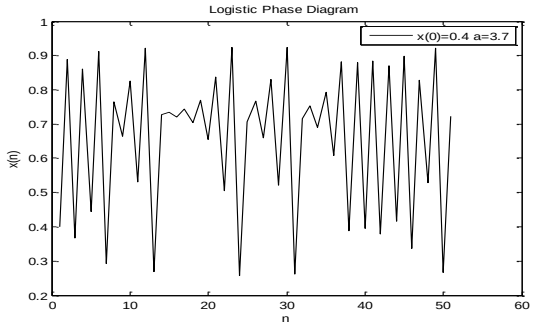

FIGURE 1 X(0)=0.4 *a*=3.7 logistic phase diagram

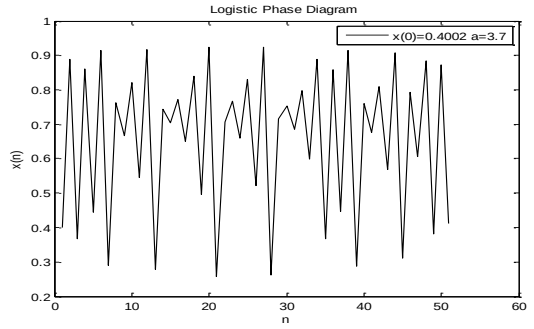

FIGURE 2 X(0)=0.4002 =3.7 logistic phase diagram

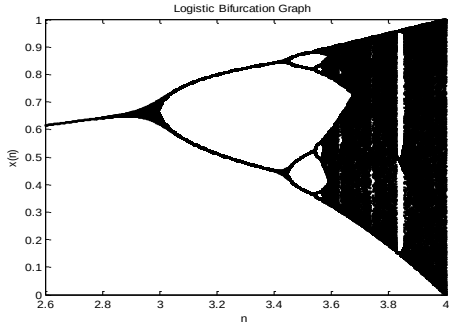

FIGURE 3 Logistic bifurcation diagram

3 Chaos differential keying communication system

Periodic signal is commonly used as the transmission carrier in the modern digital communication systems, while it has a relatively narrow bandwidth after being modulated, moreover it will be seriously declined in the transmission of multipath channel; while the chaos signal produced by the identified nonlinear System with broadband noise power spectrum and stable statistical properties. It is difficult to be deciphered and easy to be implemented, its autocorrelation function of the approximate impact is a good rejection to multipath fading, it's approximation of zero cross-correlation function can better suppress interference from other users.

So the applications of chaotic systems in communications become urgent and necessary. Previously some researchers implement it by physical analogue circuit with its complex realization causing numerous difficulties to the application and promotion; while some other researchers realize it by digital circuits which simplify the design of the system. But we use chaotic digital systems as a research method, when the input signal is a digital signal, we can take advantages of all the good features of the Chaos Shift Keying.

Chaos Shift Keying modulates parameters of chaotic systems of the sender by the sending digital signal, the parameters switch in the two values then the information is encoded in the two chaotic systems, the receiving side is of two same type of chaotic systems and its parameters were fixed to one of the two values, finally it will determine the sending information by detecting the synchronization error of chaotic systems in each interval of the information sent through. In the technology, the demodulation is generally achieved by discrimination of the error signal, and to obtain the optimal decision threshold is a little difficult. Through research, we found that to realize the strange non-chaotic attractor of synchronization the chaotic system not only can achieve the same phase synchronization also can achieve the reverse synchronization, these features are helpful for the realization of chaos shift keying.

At present, the differences between different Chaos Shift Keying are mainly in the choice of the chaotic system being synchronous or asynchronous and the detection being correlation or non-correlation. Currently the technology of the Chaos Shift Keying mainly are the superior performance Differential Chaos Shift Keying (DCSK) and FM differential keying (FM-DCSK Communication) developing from the initial chaos shift keying (CSK) and the chaos-off keying (Chaotic On-Off-Keying). Research done in this article is based DCSK chaotic communications system, in the following we will give a brief introduction of principles of DCSK keying.

3.1 INTRODUCTION OF DCSK

The initial chaos shift keying (CSK) was first proposed in 1993 by Parlitz and Dedieu, the chaotic signal as an information carrier has the ergodicity broadband aperiodic signal, its most notable feature is the sensitivity and the random to the initial value. Since then the study of chaos shift keying had developed rapidly, and the initial demodulation method was of coherent demodulation. Coherent demodulation is to use the binary (or hex) digital signal being sent chaos shift keying the chaotic signal of the transmitter, achieve synchronization of sending and receiving ends of the chaotic circuit by Synchronization method based on one-way coupling, and demodulate the signal at the receiving end according to correlation receiving. The practical application of chaos pick up since the achievement of chaos synchronization technology, but chaotic synchronization is complex, costly, and also has some impact on the communication system. In order to solve the defects of this method, Dr. G. Kolumban proposed differential chaos shift keying (DCSK) based on the differential receiver in 1966, the principle is shown in Figure 4. In this principle it does not need to consider the synchronization signal, there is no doubt that is a very important signal for stability and implementation cost of the communication system, and its ruling door limit does not depend on the signal-to-noise ratio, which will broaden

chaotic systems' application significance in communication systems.

DCSK, to send each bit signal is represented by two chaotic systems with sampling function, the first function as a reference signal, the second function is to carry the signal, send the signal "1", the second function of the signal and the reference signal in phase, the signals sent to "0", then the second function of the signal and reference signal inverting.

$$s(t)=\begin{cases} c(t) & (\mathrm{l}-1)\mathrm{T}_b \le t < (l-1/2)T_b \\ -c(t-T_b/2) & (\mathrm{l}-1/2)\mathrm{T}_b \le t < lT_b \end{cases}.$$

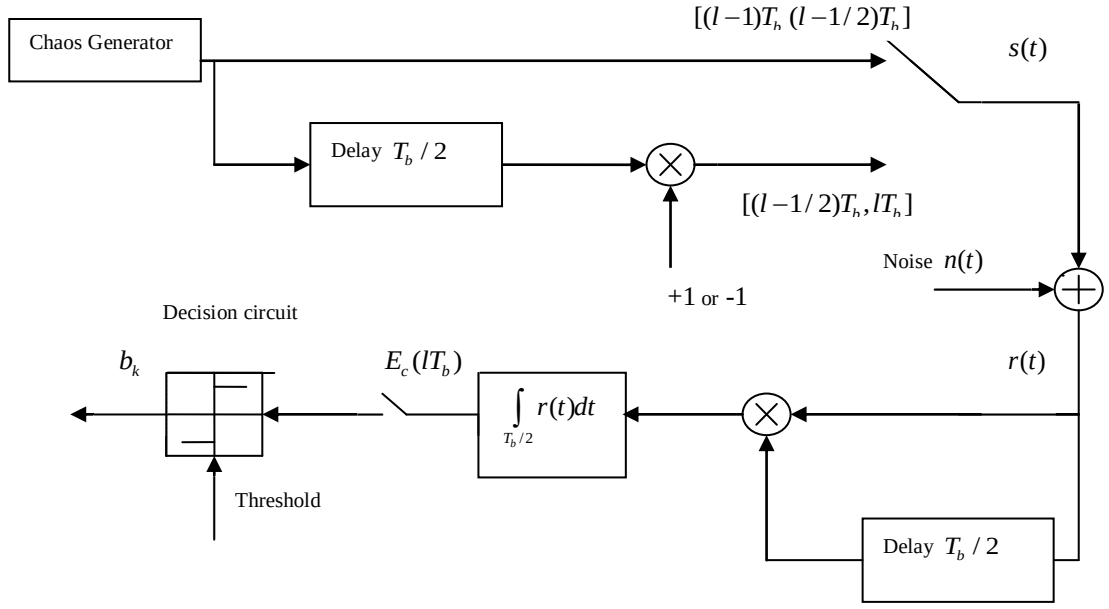

FIGURE 4 Schematic of DCSK Communication System

When the modulated signal transmits through the channel, it is interfered by the additive white Gaussian noise $n(t)$, then we demodulate it at the receiver end by completing related operation of the two kind of value function received in half code period, the output of the value related is:

$$E(lT)=\int_{(l-1/2)T}^{lT} r(t)r(t-T/2)dt=$$

$$\int_{(l-1/2)T}^{lT}[s(t)+n(t)][s(t-T/2)+n(t-T/2)]dt \;=$$

$$\int_{(l-1/2)T}^{lT}[s(t)s(t-T/2)]dt+\int_{(l-1/2)T}^{lT}[s(t)n(t-T/2)]dt+$$

$$\int_{(l-1/2)T}^{lT}[s(t-T/2)n(t)]dt+\int_{(l-1/2)T}^{lT}[n(t)n(t-T/2)]dt$$

According to DCSK modulation principle, the information sent is included in the value of the two adjacent code samples. The first item of the above equation can be plus or minus, If you send "1" it is plus; and send "0" it is minus, namely non-inverting or inverting operation on the carrier. The second, third, and fourth items are interference items, for the chaotic signal $s(t)$ and Gaussian white noise $n(t)$ are not related as well as $n(t)$ and $n(t-T/2)$. So the integral values of the second, third, and fourth items are all zero, and the decision threshold of the DCSK system is constant zero, which has nothing to do with noise ratio of the signal, which is largely enhanced its interference immunity, and also reduces the cost significantly. Moreover DCSK system uses non-coherent demodulation, avoiding the chaos synchronization problem, its feasibility is relatively high in the actual circuit, the reference signal and data signal transmit through the same channel, this kind of modulation is not sensitive to channel distortion, and can even work in the time-varying channel, with the strongest robustness.

4 FPGA and DSP builder

It is a digital prevalent era, the digital integrated circuits are widely used and are constantly upgraded from the initial tubes, transistors, small-scale integrated circuits, to ultra large scale integrated circuits, and many specific features integrated circuits. With the rapidly development of science and the times, more and more engineers and scientists hope that they can quickly design digital integrated circuits in accordance with their wishes in their own laboratories, so it will be easier to match the device and improve the efficiency of the secondary development, finally it give rise to the field programmable gate array (FPGA) and complex programmable logic device (CPLD).

At the beginning, there are only three kinds of programmable logic devices programmable read-only memory, ultraviolet ray read-only memory and electrical erasable read-only memory. Due to the structural limitations, they can only achieve some simple logic functions, limiting the use. After the continuous efforts of the long-term scientific research in the field of the workers, it give rise to a class of structurally complex programmable chips can be programmed (PLD), the performance of the complex program-

mable chip is better than pre-programmable devices and it can complete a variety of digital logic circuit design.

The generation of the PLD, to some extent, promotes the development of new digital integrated circuits. At this stage the main products are PAL (programmable array logic) and GAL (generic array logic). PAL consists of a programmable "and" plane and a fixed "or" flat composition, the output of the "or" gate can be triggered selectively to set the storage state. PAL devices are field-programmable with anti-fuse technology, EPROM and EEPROM technology. There are some of the more flexible structure logic devices, for example programmable logic array (PLA), it consists of two flat a "and" plane and a "or" plane and their connection is programmable. There are field-programmable PLA device also mask programmable. There also emerges the generic array logic GAL on the basis of the PLA But these early PLD devices can only achieve some small-scale logic circuits due to its simplistic structure.

By the 1980s, Altera and Xilinx introduced similar to the expansion of the PLA structure CPLD and FPGA similar to the standard gate array, they both have a flexible architecture and logic unit, high integration, as well as for a wide range of application characteristics. The emerge of this kind devices promote the development of large-scale programmable logic circuits. With the development of the FPGA system-level design of digital circuits has been accepted by the researchers.

FPGA (Field-Programmable Gate Array), it is a product developed on the basis of PAL, GAL, CPLD and other programmable devices. It appears as the field of application specific integrated circuit (ASIC) in a semi-custom circuit, which addresses the lack of custom circuits, also overcomes the original programmable devices gate' shortcoming the limited number. Which provides an ideal testing ground for the development and implementation of sub-electronic systems, then the developers do not need to custom hardware for the designs not-tested, which not only reduces the development costs but also improves the speed of development, and provides great flexibility for the development process to modify the hardware and debugging.

It requires advanced algorithms and hardware description language (VHDL) development tools in the digital signal processing (DSP) system design by the Altera programmable logic devices (PLDs). The Altera DSP Builder integrates these tools and combines the MathWorks MATLAB/Simulink system-level design tools for algorithm development, simulation and verification capabilities, and VHDL and Verilog design flow (including Altera's Quartus II software) together, which to a certain extent shows the trend of modern EDA technology in the development and application. We can translate the Simulink model involved in directly into hardware description language available to be downloaded to FPGA, providing a great convenience.

5 Design of chaotic differential keying communication system based on DSP builder

The DCSK system built in the DSP Builder inside is shown in Figure 5, the following give a detailed description of its all aspects.

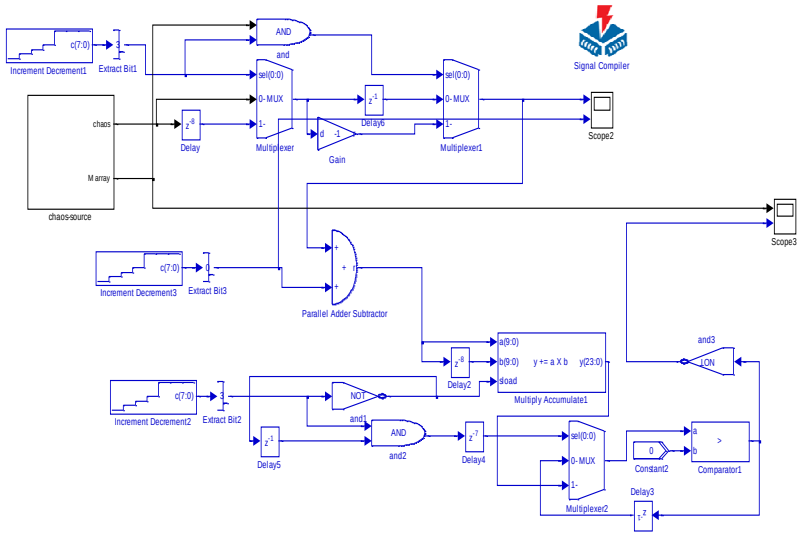

FIGURE 5 The whole DCSK system built in DSP Builder

5.1 THE GENERATING UNIT OF CHAOTIC SIGNAL

In this paper, we use the Logistic model as a chaotic signal source, and its mathematical model is

$$X_{n+1}=\mu X_n(1-X_n).$$

The block diagram built in DSP Builder are as shown below in Figure 6.

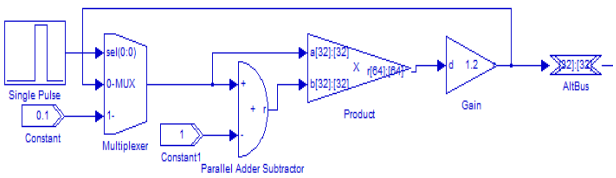

FIGURE 6 The chaotic model constructed by DSP the builder

The output Logistic chaotic signal through the built the model, its output waveform is as shown in Figure 7.

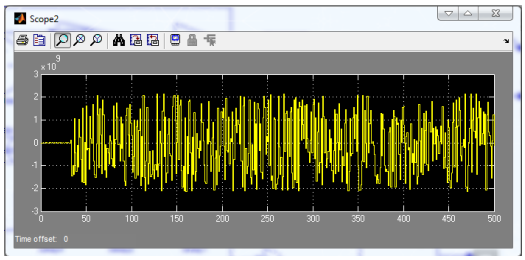

FIGURE 7 The chaotic model waveform constructed by DSP builder

5.2 THE DESIGN OF TRANSMITTER

As it is shown in Figure 8 the transmitter modulation principle, the sending module consists of the chaotic signal source and binary DCSK modulator, the former is a chaotic source, the latter is a modulator including the switching circuit and the delay unit etc.

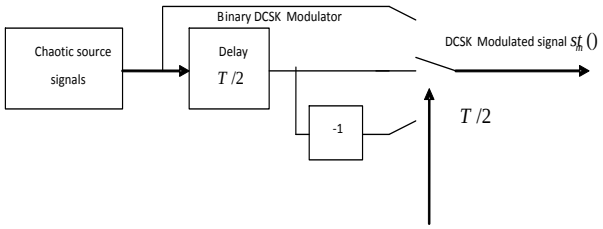

FIGURE 8 DCSK Communication modulation principle

Binary DCSK Modulation method is to use the transmission signal binary "0" and "1" to switch keying output chaotic signal. The chaotic signal transmitted in the last $T/2$ is a delay of $T/2$ of the chaotic signal transmitted in the first $T/2$, and controlled by the digital signal to be transmitted. Eventually modulating the signal to be transmitted into the chaotic signal; If the transmitted signal is "1", the chaotic signal transmitted before and after the first $T/2$ modulated signal time is with the same phase; if the transmitted signal is "0", the chaotic signal transmitted before and after the first $T/2$ modulated signal time is with the anti-phase.

It is because of this the clock signal start with the low level, then in the first $T/2$ it needs to keep the output signal all remaining the original. If the two selector switch are both the 0 channel, then the control sides are all low; So it can achieve control of the second selector switch by take the signal to be transmitted and the clock phase part through and gate, so with an and gate and two selector switches we can complete the signal modulation process.

DCSK Modulation DSP Builder block diagram in Figure 9.

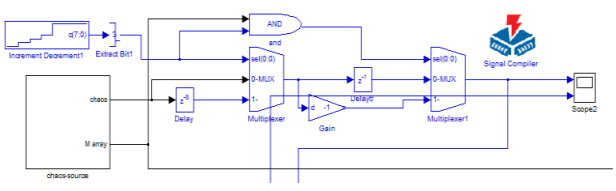

FIGURE 9 The modulation link built in DSP Builder

5.3 THE DESIGN OF THE RECEIVER

In this system we use modules of the product of cumulative to achieve digital integrator, according to features of integral module of the DSP Builder, we need to complete the cumulative output when the sload console input are high, and restore it by cumulating output after the "0" decision threshold (Figure 10).

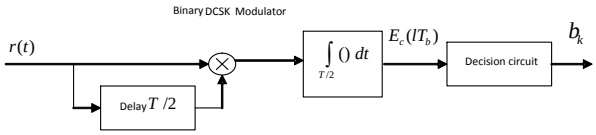

FIGURE 10 DCSK communication demodulation

DSP Builder block diagram in Figure 11 for the receiver design:

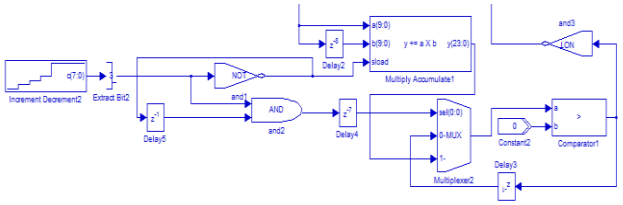

FIGURE 11 DSP Builder build demodulation link

5.4 THE ANALYSIS OF THE SYSTEM SIMULATION RESULTS

After building the system we carry out the simulation. In Figure 12, it is the waveform of the data flow route of the simulation process.

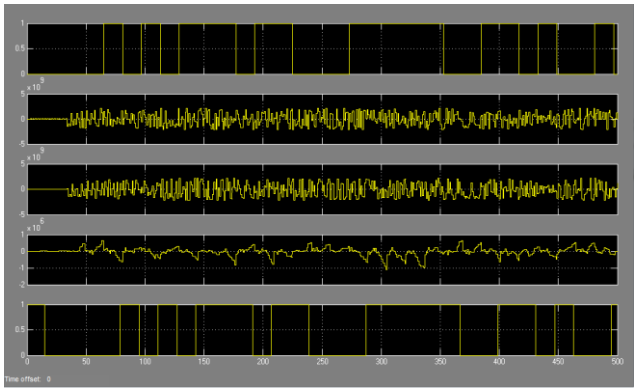

FIGURE 12 The signal comparison before and after modulation

The first waveform is the digital signal wave required to be transmitted M signal to generate random signal. It is conducive to the inspection system of the general performance. The second waveform is a chaotic carrier signal wave, from the waveform it can be seen the disorder of the Logistic chaotic signal, it reflects the performance of the confidentiality of the communication system, and it is not easy to be cracked. The third waveform is the transmitted signal modulated into the chaotic carrier wave, by comparing with the chaotic signal un-modulated, though a bit different, the waveform is displayed disorganized, compa-

rison of the two wave shows the confidentiality of the chaotic communication. The fourth waveform signals is the signal wave from the transmission signal to the receiver digital integration, if the signal transmitted is high, the signal before and after the half-cycle is in phase, the results after the integral is greater than "0", if the signal transmitted is low, then the result is opposite, which provides a very simple method to restore the signal, it simply need to compare the integral results with "0" the reference gate limit. The last waveform is the signal restored through the judgment link by the digital integrator. It can be seen that there is a certain delay, while the signal transmitted eventually can be modulated, which to some extent shows that the chaotic signal as a carrier for signal transmission is feasible. It provides an approach for us to use DSP builder to make designs on the system-level or algorithm-level and to convert it to the corresponding hardware description language.

6 Conclusion

This paper is based on modern digital signal processing technology, and implement chaos shift keying communications technology through DSP builder software design. It is easy to adjust the various parameters of the circuit, it is better than using the traditional analog circuit, the method overcomes the design difficulty and instability of the chaos shift keying designed through analog circuits, while it easy to modify the parameters, to observe the results, and to keep stable. And the discretization Chaos Shift Keying system is easier to be implemented in FPGA. We have made some experiments on chaos shift keying research, and made some analysis and comparison of the results then concluded that we can use it to maintain the confidentiality of communications through the control and synchronization of the chaotic circuit. This paper has a great signifycance of applying the chaos to actual confidential communication systems.

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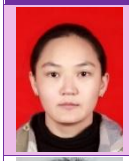

Zhiping Liu, April 11th, 1979, China.

Current position, grades: lecturer in Henan Polytechnic University.
University studies: Msc in communication and information system from Nanjing University of Posts and Communications Engineering.
Scientific interest: wireless communications, sensor network.
Publications: 2papers.

Jinhua Zhang, August 20th, 1979, China.

University studies: electronic Information science and technology
Scientific interest: process Instruments

Hanyu Liu, August 18th, 1989, China.

University studies: electronic information science and technology.
Scientific interest: wireless communications, chaotic communications.